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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of

CETIN KAYA

Serial No. 09/620,649 (TI-23686.1)

Filed July 20, 2000

For: INTEGRATED CIRCUIT HAVING INDEPENDENTLY FORMED ARRAY AND PERIPHERAL ISOLATION DIELECTRICS

Art Unit 2822

Examiner Mary A. Wilczewski

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Jay M. Cantor, Reg. No. 19,906

BRIEF ON APPEAL

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, a Delaware corporation with offices at 7839 Churchill Way, Dallas, Texas 75251.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals and/or interferences other than a prior appeal in this application.

STATUS OF CLAIMS

This is an appeal of claims 12 to 19, all of the rejected claims. Claim 20 has been allowed and claims 1 to 11 were the subject of the parent application. Please charge any costs to Deposit Account No. 20-0668.

STATUS OF AMENDMENTS

An amendment was not filed after a second or subsequent rejection.

SUMMARY OF INVENTION

The invention relates to an integrated circuit (10) having a first dielectric layer (20) disposed outwardly from a substrate (12). A plurality of gate stacks (22) are provided, each gate stack having a floating gate body (24) disposed outwardly from the first dielectric layer, a second dielectric region (28) disposed outwardly from the floating gate body and a first polysilicon layer (26) disposed outwardly from the second dielectric region. A plurality of dielectric isolation regions (30) are disposed between the gate stacks, the dielectric isolation regions formed after the formation of the gate stacks. Each dielectric isolation region may include an isolation oxide layer (32) and an isolation dielectric layer (34), the dielectric isolation region formed by growing the isolation oxide layer outwardly from the gate stacks, depositing the isolation dielectric layer outwardly from and between the gate stacks, and removing at least a portion of the isolation oxide layer and the isolation dielectric layer to expose at least an outer surface of the first polysilicon layer. The dielectric isolation regions can be formed by growing approximately 200Å of oxide outwardly from the gate stacks, depositing approximately 0.5 micrometers of oxide outwardly from and between the gate stacks and removing at least a portion of the isolation oxide layer and the isolation dielectric

layer to expose at least an outer surface of the first polysilicon layer. Each floating gate body can have a rough outer surface.

ISSUES

The sole issue on appeal is whether appellant has properly antedated the reference to Van Buskirk et al. (U.S. 6,001,689) to remove this reference as an applicable reference under 35 U.S.C. 102 or 103 against claims 12 to 19.

GROUPING OF CLAIMS

The claims stand or fall together.

ARGUMENT

Claims 12, 13, 15 and 16 were rejected under 35 U.S.C. 102(e) as being anticipated by Van Buskirk et al. and claims 18 and 19 were rejected under 35 U.S.C. 103(a) as being unpatentable over Van Buskirk et al. in view of Woo et al. (U.S. 5,926,711). The rejections are without merit because Van Buskirk et al. is not available as a reference in this application.

Attention is invited to the Decision of the United States Supreme Court in Pfaff v Wells Electronics, 525 U.S. 55 (U.S. 1998) wherein the meaning of the term "invention" was specifically defined as it applies to 35 U.S.C.

It is clear from reading 35 U.S.C. that the word "invention" in the statute "does not contain any express requirement that an invention must be reduced to practice" as stated in Pfaff and even in section 102(g) where the conception and reduction to practice are specifically mentioned, there is no requirement that these be the only factors considered. If follows, first, that 35 U.S.C. nowhere defines "invention" by a

determination solely of the questions of reduction to practice or conception with diligence up to a reduction to practice (actual or constructive). While a proper showing of a reduction to practice or conception with diligence up to a reduction to practice does establish invention under 35 U.S.C, there is nothing in 35 U.S.C. which limits the definition of invention to only those factors. This is confirmed in Pfaff wherein the Court rejected the longstanding precedent set forth above by stating [III] "Pfaff nevertheless argues that longstanding precedent buttressed by the strong interest in providing inventors with a clear standard identifying the onset of the 1-year period, justifies a special interpretation of the word 'invention' as used in § 102(b). We are persuaded that this nontextual argument should be rejected."

As stated in the opinion in defining the term "invention", the Court states that "Thus petitioner's argument calls into question the standard applied by the Court of Appeals, but it does not persuade us that it is necessary to engraft a reduction to practice element into the meaning of the term 'invention' as used in § 102(b)."

The Court further states:

> "The word 'invention' must refer to a concept that is complete, rather than merely one that is 'substantially complete.' It is true that reduction to practice ordinarily provides the best evidence that an invention is complete. But just because reduction to practice is sufficient evidence of completion, it does not follow that proof of reduction to practice is necessary in every case. Indeed, both the facts of the Telephone Cases and the facts of this case demonstrate that one can prove that an invention is complete and ready for patenting before it has actually been reduced to practice."

The Court concluded that the on-sale bar applies when two conditions are satisfied, the first condition not being applicable in this case because it relates to conditions of sale. However, the second condition relates to the definition of "invention" and states:

> "Second, the invention must be ready for patenting. That condition may be satisfied in at least two ways: by proof of reduction to practice before the critical date; or by proof that prior to the critical date the inventor had prepared drawing or other descriptions of the invention that were sufficiently specific to enable a person skilled in the art to practice the invention. In this case the second condition of the on-sale bar is satisfied because the drawing Pfaff sent to the manufacturer before the critical date fully disclosed the invention: (underline not in original)

It follows that an invention disclosure is provided if it contains "prepared drawing or other descriptions of the invention that were sufficiently specific to enable a person skilled in the art to practice the invention".

In the present appeal, the specification in the provisional application Serial No. 60/060,561 is substantially identical to the specification in the subject application on appeal. There has never been any question of sufficiency of disclosure of the claimed invention in the prosecution of the subject application. If follows that the subject application contains a disclosure which is ready for patenting as defined by the Supreme Court in Pfaff and that appellant is entitled to rely at least upon the filing date of his provisional application (and possibly an earlier date if it can be established).

The subject application was refiled as an RCE out of an abundance of caution in view of the DECISION ON REHEARING mailed December 31, 2003 since it was not clear whether the DECISION ON REHEARING had in fact entered the new argument presented for the first time therein in view of the statement therein that "[t]he appellant's new argument based on Pfaff is not appropriate in this rehearing and is therefore unavailing". That argument is clearly appropriate and of record in this appeal.

However, the Board stated in the DECISION ON REHEARING that "Pfaff" has little, if any, relevance to the facts of the present case. That is, Pfaff did not address 37 C.F.R. 1.131 (2003) (effective Nov. 29, 2000)". This statement does not fully address the issue involved. 37 C.F.R.1.131 was not addressed specifically and was not required. However, a Declaration was filed July 23, 2001 which could and should be considered as though it is a declaration under 37 C.F.R.1.131. This declaration, considered in conjunction with the Pfaff decision, provides specific reference to the provisional application which was a demonstration of the claimed invention herein as being ready for patenting prior to the effective date of the Van Buskirk et al. reference. Furthermore, 37 C.F.R. 1.131 is only one vehicle for antedating a reference and not the only vehicle to for accomplishing this purpose. In affidavits or declarations under 37 C.F.R. 1.131, evidence not of record must be provided to prove invention prior to the effective date of a reference. In the present case, no such evidence is required since the evidence required is already of record and clearly shows a date of invention as defined by Pfaff (ready for patenting) prior to the effective date of Van Buskirk et al.. It follows that (1) the requirements of 37 C.F.R. 1.131 have been met and (2) the record herein clearly shows,

without any requirement to use 37 C.F.R. 1.131, that applicant had an invention ready for patenting prior to the effective date of Van Buskirk et al.

CONCLUSIONS

For the reasons stated above, reversal of the final rejection and allowance of the claims on appeal is requested that justice be done in the premises.

Respectfully submitted,

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APPENDIX

The claims on appeal read as follows:

12. An integrated circuit, comprising:

a first dielectric layer disposed outwardly from a substrate;

a plurality of gate stacks, each gate stack comprising:

a floating gate body disposed outwardly from the first dielectric layer;

a second dielectric region disposed outwardly from the floating gate body; and

a first polysilicon layer disposed outwardly from the second dielectric region; and

a plurality of dielectric isolation regions disposed between the gate stacks, the dielectric isolation regions disposed between the gate stacks, the dielectric isolation regions formed after the formation of the gate stacks.

13. The integrated circuit of Claim 12, wherein each dielectric isolation region comprises:

an isolation oxide layer; and

and isolation dielectric layer;

the dielectric isolation region formed by growing the isolation oxide layer outwardly from the gate stacks;

depositing the isolation dielectric layer outwardly from and between the gate stacks, and removing at least a portion of the isolation oxide layer and the isolation dielectric layer to expose at least an outer surface of the first polysilicon layer.

14. The integrated circuit of Claim 12, wherein each dielectric isolation region comprises:

an isolation oxide layer; and

an isolation dielectric layer;

the dielectric isolation region formed by:

growing approximately 200Å of oxide outwardly from the gate stacks;

depositing approximately 0.5 micrometers of oxide outwardly from and between the gate stacks; and

removing at least a portion of the isolation oxide layer and the isolation dielectric layer to expose at least an outer surface of the first polysilicon layer.

15. The integrated circuit of Claim 12, wherein the substrate comprises at least one trench disposed between two gate stacks; and

at least one moat disposed adjacent to the at least one trench and inwardly from the at least one gate stack.

16. The integrated circuit of Claim 15, wherein each dielectric isolation region comprises:

an isolation oxide layer; and

an isolation dielectric layer;

the dielectric isolation region formed by:

growing a layer of oxide outwardly from the gate stacks;

depositing a dielectric outwardly from and between the gate stacks and outwardly from the trenches in the substrate; and

removing at least a portion of the isolation oxide layer and the isolation dielectric layer to expose at least an outer surface of the first polysilicon layer.

17. The integrated circuit of Claim 12, wherein each second dielectric region comprises a layer of oxide having a thickness of approximately 70 Å.

18. The integrated circuit of Claim 12, wherein each gate stack further comprises a hemispherical grain poly layer disposed outwardly from the floating gate body.

19. The integrated circuit of Claim 12, wherein each floating gate body comprises a rough outer surface.